REMARKS

Reconsideration and allowance is respectfully requested. Before entry of this amendment, claims 1-23 were pending. In the Office Action, claims 1-23 were rejected. In the present amendment, claims 19-21 are amended. After entry of the amendment, claims 1-23 are pending.

I. Claims 1-7, 9-18 and 22-23

Claims 1-7, 9-18 and 22-23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bongiorno in view of Kemeny et al. (USP 7,062,675) (Office Action, p. 3, lines 17-19). To establish a *prima facie* case of obviousness, the Examiner must demonstrate three criteria. The MPEP § 2142 states:

> "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the reference (or references when combined) must teach or suggest all the claimed limitations." MPEP § 2142 (emphasis added).

A. Independent claim 1

The combination of Bongiorno and Kemeny does not form the basis for a valid rejection of claim 1 under § 103(a) for at least three reasons. First, the references when combined do not teach or suggest all of the claim elements. Second, there is no motivation to modify the teachings of Bongiorno with the teachings of Kemeny. And third, there is no reasonable expectation of success in modifying the teachings of Bongiorno with the teachings of Kemeny.

Claim 1 recites "(b) decoupling the first clock circuit . . . (c) coupling a second clock circuit . . . (d) enabling a third clock circuit . . . (e) decoupling the second clock circuit . . . and (f) coupling the third clock circuit . . .". Neither Bongiorno nor Kemeny teaches decoupling a first clock circuit, coupling a second clock circuit,

decoupling the second clock circuit, and coupling a third clock circuit. Moreover, neither Bongiorno nor Kemeny teaches enabling a third clock circuit.

(i) Neither reference teaches decoupling more than two clock circuits.

The Examiner states that Bongiorno teaches "(b) decoupling (deselecting via switching means 66 within 60) the first clock circuit (10) . . . (c) coupling (selecting) a second clock circuit (20) . . . (e) decouplilng (deselecting) the second clock circuit (20) . . . and (f) coupling (selecting) a third clock circuit (30) to the system clock input lead of the processor (Bongiorno discloses a third clock [30] being selected [via switching means 66 within 60] to the processor[80]; column 4, lines 2-8 and column 4, lines 22-34 and column 4, line 61 thru column 5, line 7)." (Office Action, p. 4, line 8 – p. 5, line 2) Applicants respectfully disagree. Nowhere does Bongiorno teach coupling a third clock circuit after decoupling a second clock circuit after coupling the second clock circuit after decoupling a first clock circuit. Bongiorno teaches only switching from one clock to another. The entirety of the passages of Bongiorno cited by the Examiner is reproduced below:

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signals has been received. Finally, the controller **40** provides the selected clock signal to a counter or timer **70**. It should be noted that the inventive circuit **100** maybe modified so as to provide the selected clock signal to any device that requires a clock signal in order to operate. Such a device may be a microprocessor **80** as shown in FIG. 1B, a digital signal processor, an application-specific integrated circuit, a reduced instruction set computer, or a microcontroller.

Referring again to FIG. 1A, the timer **70** may be a component of a microprocessor-based chip or an integrated circuit that also contains a microprocessor. If so, the timer **70** is preferably a watchdog timer that generates a signal to reset the microprocessor and disable the integrated circuit when the integrated circuit experiences a control failure or a lockup. In this embodiment, the programmed code received by the controller **40** designates the clock source **10** as a first choice for providing the clock signal to the timer **70**. Thus, clock sources **20** and **30** are essentially safety means from which the timer **70** secures a clock signal in order to operate when the clock source **10** becomes malfunctioned and no longer generates any clock signal.

Regarding the controller **40**, it may include a detector **50** and a clock signal selector **60**, both of which receive the clock signals from the clock sources **10**, **20** and **30**. The detector **50** generates a clock source availability signal that indicates whether the clock signals of the clock sources **10**, **20** and **30** have been received. Thereby, the clock source availability signal is provided to the clock signal selector **60** of the controller **40**. In addition, the clock signal selector **60** is programmable to choose one of the clock signals designated by the programmed code. Based on the clock source availability signal and the programmed code, the clock signal selector **60** selects the designated clock signal when the designated clock signal has been received. Otherwise, the clock signal selector **60** automatically selects one of the undesignated clock signals when the designated clock signal has not been received and when at least one of the undesignated clock signals has been received.

With respect to the detector **40**, it may include a delay circuit **54** and three logic gates **55**, **56** and **57** as illustrated by FIG. 2A. The delay circuit **54** receive first, second and third clock signals from the clock sources **10**, **20** and **30** of FIG. **1**, respectively. Similarly, the logic gates **55**, **56** and **57** receive the first, second and third clock signals, respectively. After the delay circuit **54** receives the first, second and third clock signals (e.g., see FIG. 2B), it outputs three time-delayed clock signals (e.g., see FIG. 2C) to the logic gates **55**, **56** and **57**. Then, the logic gates **55**, **56** and **57** respectively output first, second and third signals that indicate whether the first, second and third clock signals have been received, respectively. Thereby, the first, second and third signals are inputted into the clock signal selector **60** of FIG. **1**. Alternatively, the first, second and third signals may be provided to respective low pass filters (not shown) that are respectively coupled between the logic gates **55**, **56** and **57** and the clock signal selector **60** so as to output respective DC signals of the first, second and third signals as input signals to the clock signal selector **60**. In the preferred embodiment, the logic gates **55**, **56** and **57** may be either an exclusive OR gate or an exclusive NOR gate.

With respect to the clock signal selector **60**, it may include an instruction latch or instruction register **62** for storing the programmed code within the clock signal selector **60**, a decoder **64** for translating the content of the instruction register **62** to a meaningful operation or instruction, and a switching means **66** for receiving the clock signals from the clock sources **10**, **20** and **30**. Based on the received clock

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source availability signal and the received programmed code, the clock signal selector **60** generates and thereby provides a control signal to the switching means **66**. In response, the switching means outputs one of the clock signals selected by the clock signal selector to the timer **70**. In a preferred embodiment, the switching means is a multiplexer.

(Bongiorno, col. 4, line 1 – col. 5, line 7) (emphasis added). Nowhere do the passages above teach the coupling to a third clock circuit after the coupling to a second and the decoupling from a first.

In addition, just before the cited passages, Bongiorno teaches that one of the undesignated clock signals is selected. Bongiorno explains, "the controller 40 selects the designated clock signal when the controller 40 has received the designated clock signal. Otherwise, controller 40 automatically selects one of the undesignated clock signals when the designated clock signal has not been received and when at least one of the undesignated clock signals has been received" (Bongiorno, col. 3, line 62 – col. 4, line 1) (emphasis added).

Even when there are more than three alternative clock sources, Bongiorno selects only one undesignated clock signal when the designated clock signal is not available. Bongiorno explains:

> "Table 2 illustrates the priority scheme with respect to four clock sources 1-4. For example, if the instruction register of the clock signal selector receives a programmed code "01011", the decoder of the clock signal would decode this programmed code so that the clock signal selector would select the clock signal from the clock source 2 when the clock source 2 is available regardless of whether the clock sources 1, 3 and 4 are available or not. If the clock source 2 is not available, the clock signal selector would select the clock source 4 when the clock source 4 is available regardless of whether the clock sources 1 and 3 are available or not. If the clock sources 2 and 4 are not available, the clock signal selector would select the clock source 3 when the clock source 3 is available regardless of whether the clock source 1 is available or not. Only when all three clock sources 2-4 are not available, the clock signal selector would select the clock source 1." (Bongiorno, col. 7, lines 25-34)

Thus, Bongiorno does not teach (i) deselecting a first clock source (10), (ii) then selecting a second clock source (20), (iii) then deselecting the second clock source (20), and (iv) then selecting a third clock source (30), as the Examiner states.

Kemeny does not teach coupling or decoupling clock circuits. In fact, Kemeny does not mention clock circuits.

(ii) Neither reference teaches enabling a clock circuit.

The Examiner admits that "Bongiorno fails to disclose the method comprising the step: (d) enabling a third clock circuit" (Office Action, p. 5, lines 3-4). Kemeny also does not teach enabling a clock circuit. The Examiner does not state that Kemeny teaches enabling a clock circuit. In fact, Kemeny does not mention either a clock circuit or a clock signal. Instead, the Examiner states, "Kemeny teaches a cache system comprising a shutdown scheme wherein a detection logic (32) detects loss of power a backup power supply (30) is turned on when the failure is detected (column 4, lines 45-51)" (Office Action, p. 5, line 5-7).

The teachings of Kemeny on how to turn on a backup power supply does not teach how to enable a clock circuit. The Examiner impermissibly construes the claim terms "enabling a third clock circuit" so broadly as to cover turning on a power supply. The Examiner's interpretation of "enabling a third clock circuit" is not consistent with either the plain and ordinary meaning of "enabling a clock circuit", or with any special meaning imparted to the term in the specification.

(iii) There is no motivation to modify the clock selection circuit of Bongiorno with the cache system shutdown scheme of Kemeny.

The Examiner states that "one of ordinary skill in the art would be motivated to make this combination of enabling/powering back-up circuits when needed after detecting a failure of a primary circuit in view of the teachings of Kemeny, as doing so would give the added benefit of providing a reliable cache flushing system to prevent system failure when a power loss is detected (as taught by Kemeny above)" (Office Action, p. 5, lines 14-18).

Applicants contend that providing a reliable cache flushing system has nothing to do with the clock selection circuit of Bongiorno and cannot serve as a recognized motivation to combine Kemeny with Bongiorno for purposes of § 103(a). Nowhere does Bongiorno suggest that providing a reliable cache flushing system was ever a consideration in providing a reliable clock signal to a device that requires a clock signal in order to operate. Providing a reliable cache flushing system and providing a reliable clock signal may not even be in the

same field of endeavor. One of skill in the art seeking to solve the problem of loss of a clock signal would not look to a reference on a cache flushing system for the solution.

In addition, Bongiorno does not deal with the problem of line power failure, and Kemeny does not deal with the problem of loss of a clock signal.

(iv) There would be no reasonable expectation of success in modifying the clock selection circuit of Bongiorno with turning on back-up power as taught by Kemeny.

The Examiner states that "It would have been obvious to one of ordinary skill of the art having the teachings of Bongiorno and Kemeny at the time the invention was made, to modify the clock switching method of Bongiorno to include the ability to enable (power on) back-up circuits when the primary fail is detected as taught by Kemeny such that when a primary clock fails the back-up replacement clock is enabled (powered-on) before use" (Office Action, p. 5, lines 10-14). Applicants respectfully disagree. It would not have been obvious to modify the clock selection method of Bongiorno to include the teachings of Kemeny on turning on battery back-up power when the primary clock of Bongiorno fails because there would be no expectation of success.

At the time the invention was made, those of skill in the art recognized that turning on a back-up clock is much more complicated than turning on battery power. The specification explains:

> "The process of switching from one clock source to another without introducing glitches onto the system clock input lead is explained in detail in connection with switching the clock source from the tertiary clock signal TerClk to the faster secondary clock signal SecClk in period 15 in figure 8A." (Specification, paragraph [0048]) (emphasis added)
> "As a consquence, each of clock select signals A3, B3 and N3 is now deasserted. Clock multiplexer 40 therefore selects ground potential on multiplexer data input lead 60. SysClk on system clock input lead 20 of processor 15 is therefore held low. By holding SysClk low while switching to a new clock source, clock controller 16 prevents an extremely short cycle from occurring between the last falling edge of the old clock (TerClk) and the first rising edge of

> the new clock (SecClk). The clock source used to clock processor 15 is therefore switched without introducing glitches onto system clock input lead 20." (Specification, paragraph [0051]) (emphasis added)

One such method for turning on a back-up clock is claimed in claim 10.

Kemeny teaches only that upon detecting a power failure, "the failure detection logic 32 causes the battery back-up power to turn on . . ." (Kemeny, col. 4, lines 49-50). Kemeny provides no detail on how battery back-up power is turned on. From this sparse teaching of turning on battery back-up power, there would be no reasonable expectation of success in trying to solve the problem of the loss of a clock signal. Moreover, this sparse teaching of turning on battery back-up power would not teach one of skill in the art how to enable a replacement clock after a primary clock fails.

The combination of Bongiorno and Kemeny does not form the basis for a valid rejection of claim 1 under § 103(a) because (i) Bongiorno and Kemeny do not teach coupling and decoupling more than two clock circuits, (ii) Bongiorno and Kemeny do not teach enabling a clock circuit, (iii) there is no motivation to modify the clock selection circuit of Bongiorno with the cache system shutdown scheme of Kemeny, and (iv) there would be no reasonable expectation of success in modifying the clock selection circuit of Bongiorno with turning on back-up power as taught by Kemeny. Reconsideration of the § 103(a) rejection and allowance of claim 1 are requested.

B. Dependent claims 2-7, 9-10 and 22-23

Claim 10 recites, "wherein a third data input lead of the multiplexer is grounded, and wherein between step (b) and step (c) the multiplexer couples the third data input lead of the multiplexer to the system clock input lead" (emphasis added). The Examiner states that Bongiorno teaches "wherein a third data input lead of the multiplexer is grounded . . . wherein between step (b) and step (c) the multiplexer couples the third data input lead of the multiplexer to the system clock

input lead (column 4, line 61 thru column 4[5], line 7)" (Office Action, p. 7, lines 19-21). Bongiorno does not teach that a grounded data input lead of a multiplexer is coupled to a system clock input lead between decoupling a first clock circuit and coupling a second clock circuit. The passage of Bongiorno cited by the Examiner mentions nothing of grounding a system clock input lead after an inadequate clock is decoupled and before a replacement clock is coupled.

In addition to the reasons states above, claims 2-7, 9-10 and 22-23 depend from claim 1 and are allowable for at least the same reasons for which claim 1 is allowable. Reconsideration of the § 103(a) rejection and allowance of claims 2-7, 9-10 and 22-23 are requested.

C. Independent claim 11

The combination of Bongiorno and Kemeny does not form the basis for a valid rejection of claim 11 under § 103(a) for at least three reasons. First, neither Bongiorno nor Kemeny teaches turning on a clock circuit upon detecting that another clock circuit has failed. Second, there is no motivation to modify the teachings of Bongiorno with the teachings of Kemeny. And third, there is no reasonable expectation of success in modifying the teachings of Bongiorno with the teachings of Kemeny.

(i) Neither reference teaches a clock controller adapted to turn on a clock circuit.

The Examiner admits that Bongiorno fails to disclose a clock controller adapted to turn on a third clock circuit. (Office Action, p. 9, lines 1-2) The Examiner does not state that Kemeny teaches turning on a clock circuit upon detecting that another clock circuit has failed. In fact, Kemeny does not mention either a clock circuit or a clock signal. Instead, the Examiner states, "Kemeny teaches a cache system comprising a shutdown scheme wherein a detection logic (32) detects loss of power a backup power supply (30) is turned on when the failure is detected (column 4, lines 45-51)" (Office Action, p. 9, line 3-5).

The teachings of Kemeny on how to turn on a backup power supply does

not teach how to turn on a clock circuit upon detecting that another clock circuit has failed. The Examiner impermissibly construes the claim terms "adapted to turn on the third clock circuit" so broadly as to cover turning on a power supply. The Examiner's interpretation of "adapted to turn on the third clock circuit" is not consistent with either the plain and ordinary meaning of "adapted to turn on the third clock circuit", or with any special meaning imparted to the term in the specification.

(ii) There is no motivation to modify the clock selection circuit of Bongiorno with the cache system shutdown scheme of Kemeny.

The Examiner states that "one of ordinary skill in the art would be motivated to make this combination of enabling/powering back-up circuits when needed after detecting a failure of a primary circuit in view of the teachings of Kemeny, as doing so would give the added benefit of providing a reliable cache flushing system to prevent system failure when a power loss is detected (as taught by Kemeny above)" (Office Action, p. 9, lines 12-16).

Applicants contend that providing a reliable cache flushing system has nothing to do with the clock selection circuit of Bongiorno and cannot serve as a recognized motivation to combine Kemeny with Bongiorno for purposes of § 103(a). Nowhere does Bongiorno suggest that providing a reliable cache flushing system was ever a consideration in providing a reliable clock signal to a device that requires a clock signal in order to operate. Providing a reliable cache flushing system and providing a reliable clock signal may not even be in the same field of endeavor. One of skill in the art seeking to solve the problem of loss of a clock signal would not look to a reference on a cache flushing system for the solution.

In addition, Bongiorno does not deal with the problem of line power failure, and Kemeny does not deal with the problem of loss of a clock signal.

(iii) There would be no expectation of success in modifying Bongiorno's clock selection circuit with Kemeny's turning on back-up power.

The Examiner states that "It would have been obvious to one of ordinary

skill of the art having the teachings of Bongiorno and Kemeny at the time the invention was made, to modify the clock switching method of Bongiorno to include the ability to enable (power on) back-up circuits when the primary fail is detected as taught by Kemeny such that when a primary clock fails the back-up replacement clock is enabled (powered-on) before use" (Office Action, p. 9, lines 8-12). Applicants respectfully disagree. It would not have been obvious to modify the clock selection method of Bongiorno to include the teachings of Kemeny on turning on battery back-up power when the primary clock of Bongiorno fails because there would be no expectation of success.

At the time the invention was made, those of skill in the art recognized that turning on a back-up clock is much more complicated than turning on battery power. The specification discloses one method of turning on a back-up clock. (See Specification, paragraphs [0048] and [0051]) A method for turning on a back-up clock is also claimed in claim 10. Kemeny teaches only that upon detecting a power failure, "the failure detection logic 32 causes the battery back-up power to turn on . . ." (Kemeny, col. 4, lines 49-50). Kemeny provides no detail on how battery back-up power is turned on. From this sparse teaching of turning on battery back-up power, there would be no reasonable expectation of success in trying to solve the problem of the loss of a clock signal. Moreover, this sparse teaching of turning on battery back-up power would not teach one of skill in the art how to make a clock controller adapted to turn on a replacement clock circuit upon detecting that the primary clock has failed.

Therefore, the combination of Bongiorno and Kemeny does not form the basis for a valid rejection of claim 11 under § 103(a) because (i) neither Bongiorno nor Kemeny teaches a clock controller adapted to turn on a replacement clock circuit upon detecting that the primary clock has failed, (ii) there is no motivation to modify the clock selection circuit of Bongiorno with the cache system shutdown scheme of Kemeny, and (iii) there would be no reasonable expectation of success in modifying the clock selection circuit of

Bongiorno with turning on back-up power as taught by Kemeny. Reconsideration of the § 103(a) rejection and allowance of claim 11 are requested.

D. Dependent claims 12-18

Claims 12-18 depend directly or indirectly from claim 11 and are allowable for at least the same reasons for which claim 11 is allowable. Reconsideration of the § 103(a) rejection and allowance of claims 12-18 are requested.

II. Claims 19-21

A. Independent claim 19

Claim 19 is rejected under 35 U.S.C. § 102(b) as being anticipated by Bongiorno et al. (USP 6,292,045) (Office Action, p. 2, lines 12-13). Claim 19 as amended recites, "wherein the means turns on the third clock circuit upon detecting that the first clock signal is inadequate". The Examiner admits that Bongiorno fails to disclose a clock controller adapted to turn on a third clock circuit. (Office Action, p. 9, lines 1-2) In addition, the Examiner admits that "Bongiorno fails to disclose the method comprising the step: (d) enabling a third clock circuit" (Office Action, p. 5, lines 3-4).

Moreover, for the reasons stated above with regard to claim 11, the combination of Bongiorno and Kemeny does not form a basis for a valid rejection of claim 19 under § 103(a).

B. Dependent claims 20-21

Claims 20-21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bongiorno in view of Kemeny (Office Action, p. 11, lines 4-5; p. 12, lines 1-2). Claims 20-21 include the following limitations of base claim 19, "wherein the means turns on the third clock circuit upon detecting that the first clock signal is inadequate". Claims 20-21 are allowable for the same reasons that amended claim 19 is allowable. Bongiorno and Kemeny do not form the basis for a valid rejection of claims 20 and 21 under § 103(a) because neither

Bongiorno nor Kemeny teaches a means that turns on a replacement clock circuit upon detecting that a primary clock signal is inadequate.

Reconsideration of the § 103(a) rejection and allowance of claims 20-21 are requested.

III. Claim 8

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Bongiorno in view of Kemeny in further view of Ohlenbusch et al. (US Pat. Pub. 2002/0091785) (Office Action, p. 12 lines 3-5).

The 3-way combination of Bongiorno, Kemeny and Ohlenbusch does not form the basis for a valid rejection of claim 8 under § 103(a) because none of Bongiorno, Kemeny or Ohlenbusch teaches (i) all of the limitations of base claim 1, or (ii) the additional limitations of claim 8.

Claim 8 includes the following limitations of base claim 1, "enabling a third clock circuit". None of Bongiorno, Kemeny or Ohlenbusch teaches enabling a clock circuit. For the reasons stated above with regard to claim 1, neither Bongiorno nor Kemeny teaches enabling a clock circuit. The teachings of Kemeny on how to turn on a backup power supply does not teach how to enable a clock circuit. Kemeny does not even mention a clock circuit or a clock signal. Ohlenbusch also does not teach enabling or turning on a clock circuit.

In addition to the limitations of base claim 1, claim 8 recites "disabling a failure detection circuit that performed the detecting in (a)", where (a) of the base claim 1 recites "detecting whether a first clock signal is inadequate". The Examiner states that Ohlenbusch teaches "an intelligent data network wherein devices that are unnecessary are turned off so as save power in the system (paragraph 36, lines 11-16)" (Office Action, p. 12, lines 7-8). The Examiner has not established a *prima facie* case of obviousness because the Examiner has not stated that Ohlenbusch teaches disabling a circuit that detects whether a clock signal is inadequate. The teaching in Ohlenbusch of nodes powering down when not transmitting or receiving messages (Ohlenbusch, paragraph [0037]) does not

teach disabling a failure detection circuit. Ohlenbusch does not teach a circuit that detects whether a clock signal is inadequate. Ohlenbusch does not even mention a failure detection circuit of any kind.

In addition, the 3-way combination of Bongiorno, Kemeny and Ohlenbusch does not form the basis for a valid rejection of claim 8 under § 103(a) because there is no motivation to modify the clock selection circuit of Bongiorno with the cache system shutdown scheme of Kemeny as well as with the intelligent data network of Ohlenbusch that reduces power consumption by powering down nodes when not transmitting or receiving messages. One of skill in the art seeking to solve the problem of loss of a clock signal would not look for the solution in a reference on a cache flushing system as well as in another reference that teaches "persistently turning devices on and off in a communication system" (Office Action, p. 12, lines 18-19).

Reconsideration of the § 103(a) rejection and allowance of claim 8 are requested.

IV. Conclusion

In view of the foregoing amendments and remarks, Applicants respectfully submit that the entire application (claims 1-23 are pending) is in condition for allowance. Applicants respectfully request that a timely Notice of Allowance be issued in this case. If the Examiner would like to discuss any aspect of this application, the Examiner is requested to contact the undersigned at (925) 550-5067.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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